Transistor Biasing

Nafees Ahamad

Asstt. Prof., EECE Deptt, DIT University, Dehradun

Website: www.eedofdit.weebly.com

Introduction

- The basic function of transistor is to do amplification. (CE connection)
- *We should have faithful* Amplification.
  (change in amplitude but not in shape)
- For this
- Input circuit (*i.e.* B-E junction) of the transistor always remains forward biased*
- output circuit (*i.e.* C-B junction) always remains always reverse biased*

*Irrespective of input signal

Faithful Amplification

- *Raising the strength of a weak signal without any change in its shape*: **Faithful Amplification**
- for achieving faithful amplification, following basic conditions must be satisfied :
- (*i*) Proper zero signal collector current
- (*ii*) Minimum proper base-emitter voltage (V_{BE}) at any instant (V_{BE}>0.5V for Ge & >0.7V for Si transistor)
- (*iii*) Minimum proper collector-emitter voltage (V_{CE}) at any instant (V_{CE}>0.5V for Ge & >1V for Si transistor)

To ensure I/p ckt is always forward biased

To ensure O/p ckt is always reverse biased

Fulfilment of these conditions is known as transistor biasing.

Transistor Biasing

- Fulfilment of above conditions is known as transistor biasing.

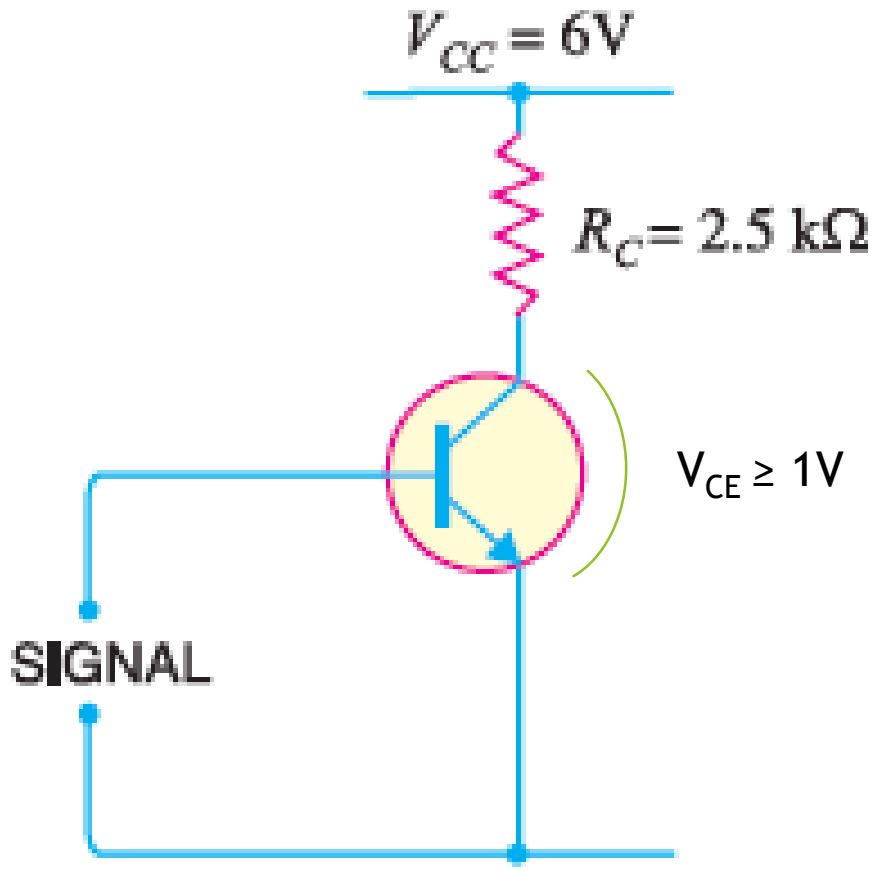
Question on Transistor Biasing

- *Q1. An npn silicon transistor has VCC = 6 V and the collector load R_C = 2.5 kΩ. Find :*
- *(i) The maximum collector current that can be allowed during the application of signal for faithful amplification.*
- *(ii) The minimum zero signal collector current required.*

Question on Transistor Biasing…

- **Solution:**
- (***i***) We know that for faithful amplification, V_{CE} should not be less than 1V for silicon transistor.
- ∴ Max. voltage allowed across R_C = 6 − 1 = 5 V
- ∴ Max. allowed collector current = 5 V/R_C = 5 V/2.5 kΩ = **2 mA**
- Thus, the maximum collector current allowed during any part of the signal is 2 mA.
- If the collector current is allowed to rise above this value, V_{CE} will fall below 1 V.

Question on Transistor Biasing…



Question on Transistor Biasing…

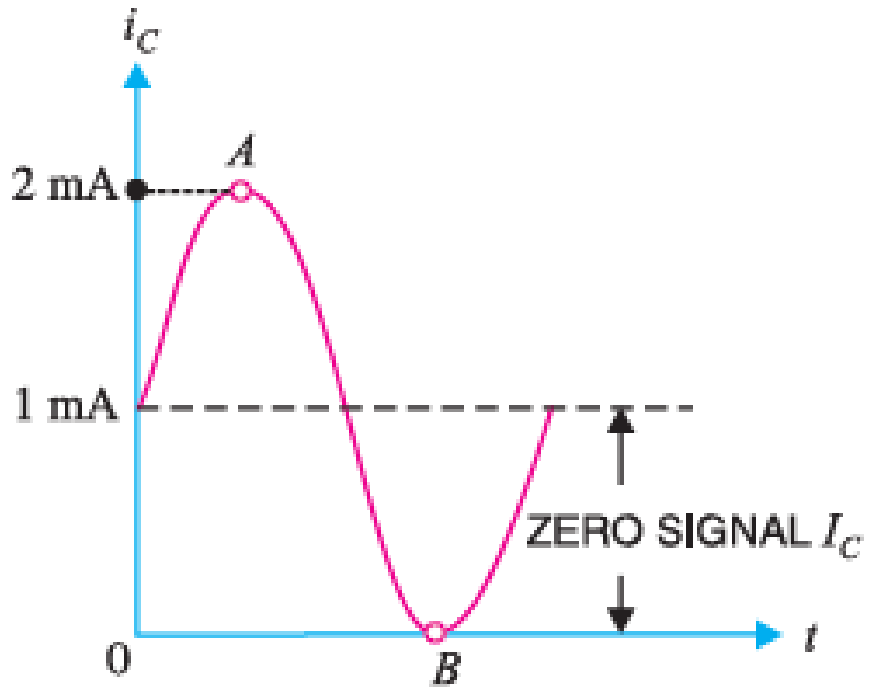
- (*ii*) During the negative peak of the signal, collector current can at the most be allowed to become zero.

  (see figure on next slide)

- As the negative and positive half cycles of the signal are equal, therefore, the change in collector current due to these will also be equal but in opposite direction.

- ∴ Minimum zero signal collector current required = 2 mA/2 = **1 mA**

Question on Transistor Biasing…



Question on Transistor Biasing…

- During the positive peak of the signal (Point A in above figure)
- i_C = 1 + 1 = 2mA
- During the negative peak (point *B* in above figure),
- i_C = 1 – 1 = 0 mA

Inherent Variations of Transistor Parameters

- In practice, the transistor parameters such as ß, V_{BE} are not the same for every transistor even of the same type.
- The major reason for these variations is that transistor is a new device and manufacturing techniques have not too much advanced.
- The inherent variations of transistor parameters may change the operating point, resulting in unfaithful amplification.
- So the operating point should be independent of transistor parameters variations.

Stabilisation

- The collector current in a transistor changes rapidly when
- (***i***) the temperature changes,
- (***ii***) the transistor is replaced by another of the same type. This is due to the inherent variations of transistor parameters.
- Due to above the operating point (*i.e.* zero signal I_C and V_{CE}) also changes.
- Stabilisation means to keep the operating point fixed i.e. independent of above changes

Stabilisation…

- **Need for Stabilisation:** Stabilisation of the operating point is necessary due to the following reasons :
- **(*i*) Temperature dependence of I_C:** The collector leakage current I_{CBO} is greatly depends on temperature, so I_C.
- **(*ii*) Individual variations:** parameters of any two transistor are not same.
- **(*iii*) Thermal runaway:** I_{CBO} keeps on increasing due to temp rise if operating point is not fixed, which result in thermal runaway of transistor.

Essentials of a Transistor Biasing Circuit

- The biasing network should meet the following requirements
- (i) It should ensure proper zero signal collector current.
- **(*ii*)** It should ensure that V_{CE} does not fall below 0.5 V for *Ge* transistors and 1 V for silicon transistors at any instant.
- **(*iii*)** It should ensure the stabilisation of operating point.

Stability Factor

- *The rate of change of collector current I_C w.r.t. the collector leakage current I_{CBO} (I_{CO}) at constant* Ɓ *and I_B is called* stability factor(S)

$$S = \frac{dI_C}{dI_{CO}} \text{ at constant } I_B \text{ and } \beta$$

- "S" should be as low as possible (ideally 1, practically <25)

Stability Factor…

- For C.E. configuration

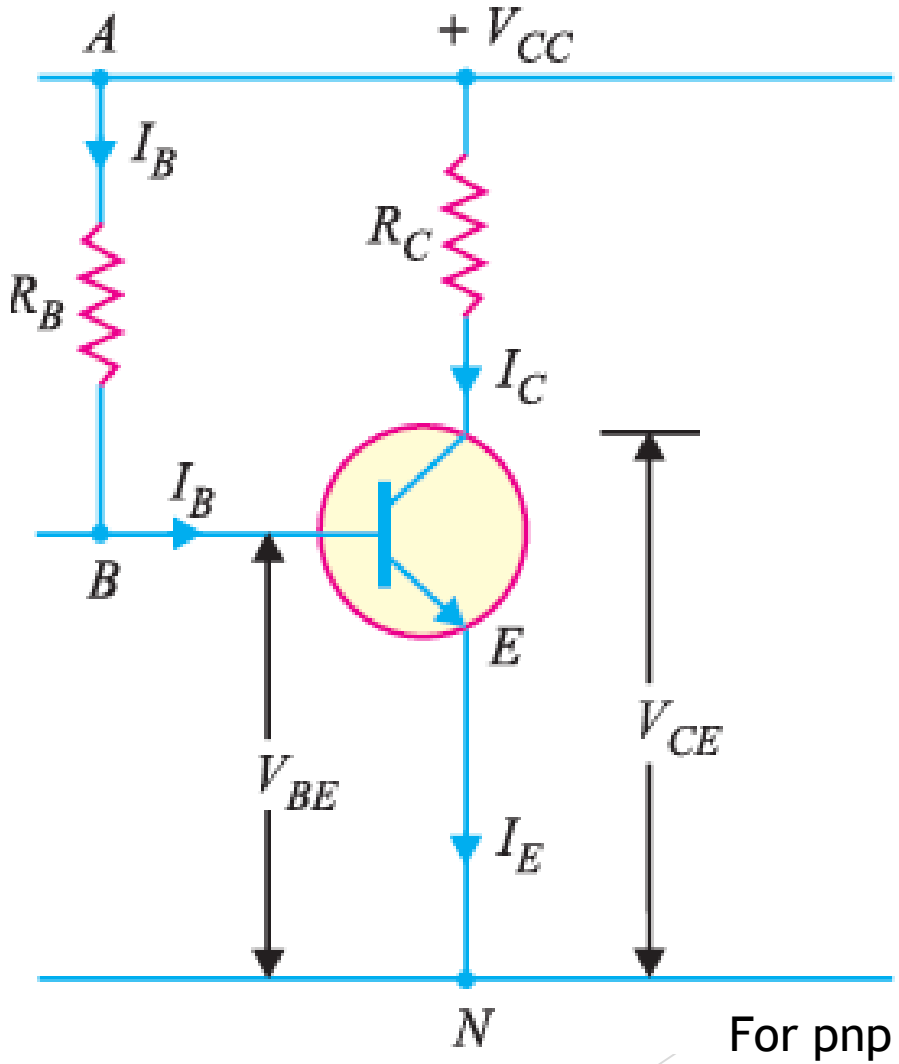
$$S = \frac{\beta + 1}{1 - \beta\left(\frac{dI_B}{dI_C}\right)}$$

Methods of Transistor Biasing

- For simplicity and economy reason, single battery can be used for biasing of both i/p and o/p circuits
- The following are the most commonly used methods of obtaining transistor biasing from one source of supply (*i.e. VCC*):
- (***i***) Base resistor method (fixed Bias)
- (***ii***) Emitter bias method
- (***iii***) Biasing with collector-feedback resistor
- (***iv***) Voltage-divider bias

Base resistor method

- A high resistance R_B (several hundred kΩ) is connected between the base and +ve end of supply forr *npn and between base and -ve end suppy for pnp* transistor.



For pnp transistor

Base resistor method…

- **Circuit analysis:** Find the value of R_B so that required collector current flows in the zero signal conditions.
- Let I_C be the required zero signal collector current.

$$\therefore \qquad I_B = \frac{I_C}{\beta}$$

- Considering the closed circuit *ABENA* and applying KVL, we get,

$$V_{CC} = I_B R_B + V_{BE} \qquad \Rightarrow \quad R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

V_{BE} is very small so may be neglected sometimes

Base resistor method…

- **Stability factor:**

$$S = \frac{\beta + 1}{1 - \beta\left(\frac{dI_B}{dI_C}\right)}$$

- In fixed-bias method of biasing, I_B is independent of I_C so that $dI_B/dI_C = 0$.
- So $S = \beta + 1$

Base resistor method…

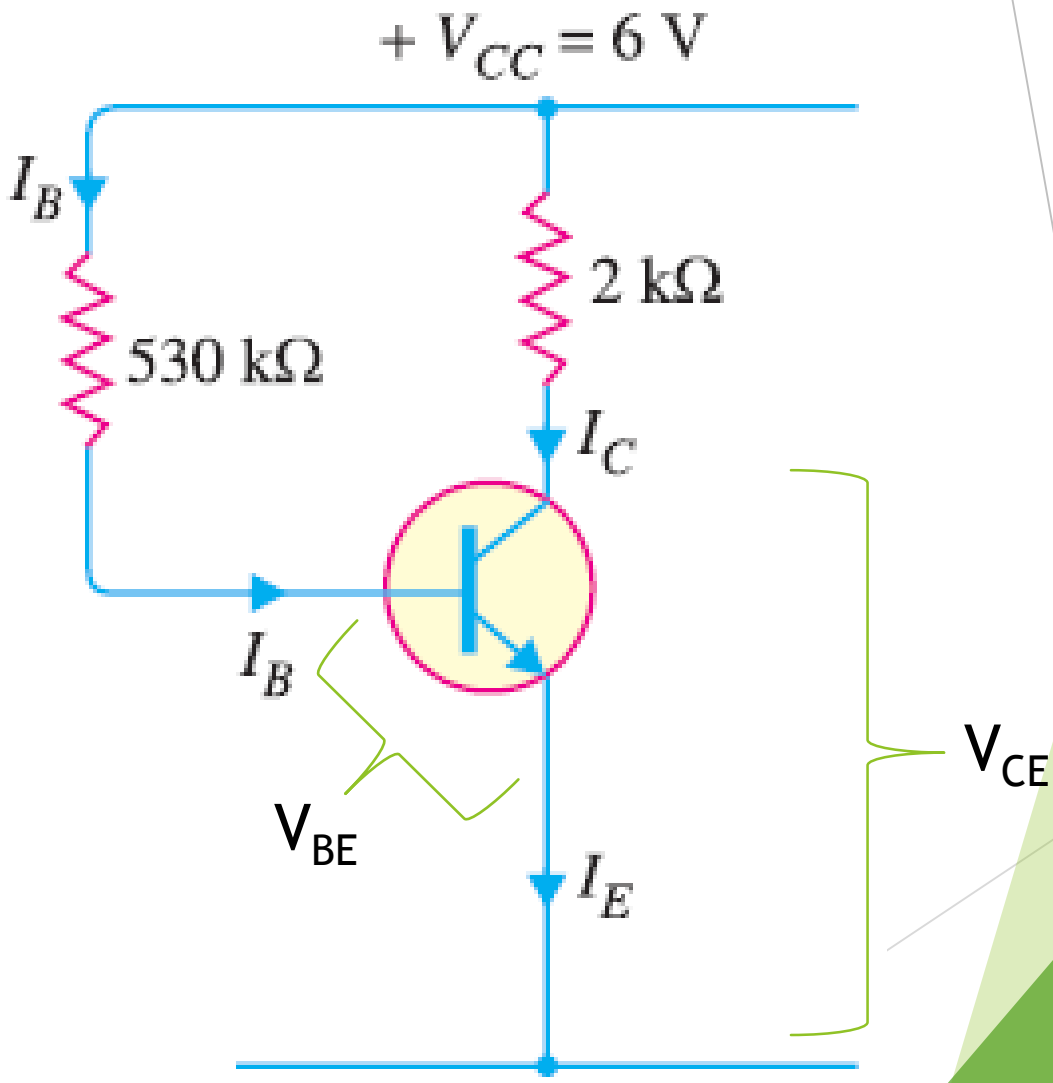
- **Advantages:**
- (***i***) This biasing circuit is very simple as only one resistance R_B is required.
- (***ii***) Biasing conditions can easily be set and the calculations are simple.
- (***iii***) There is no loading of the source by the biasing circuit since no resistor is employed across base-emitter junction.

Base resistor method…

- **Disadvantages :**
- (***i***) This method provides poor stabilisation.
- (***ii***) The stability factor is very high (chances of thermal runaway.)

Base resistor method…

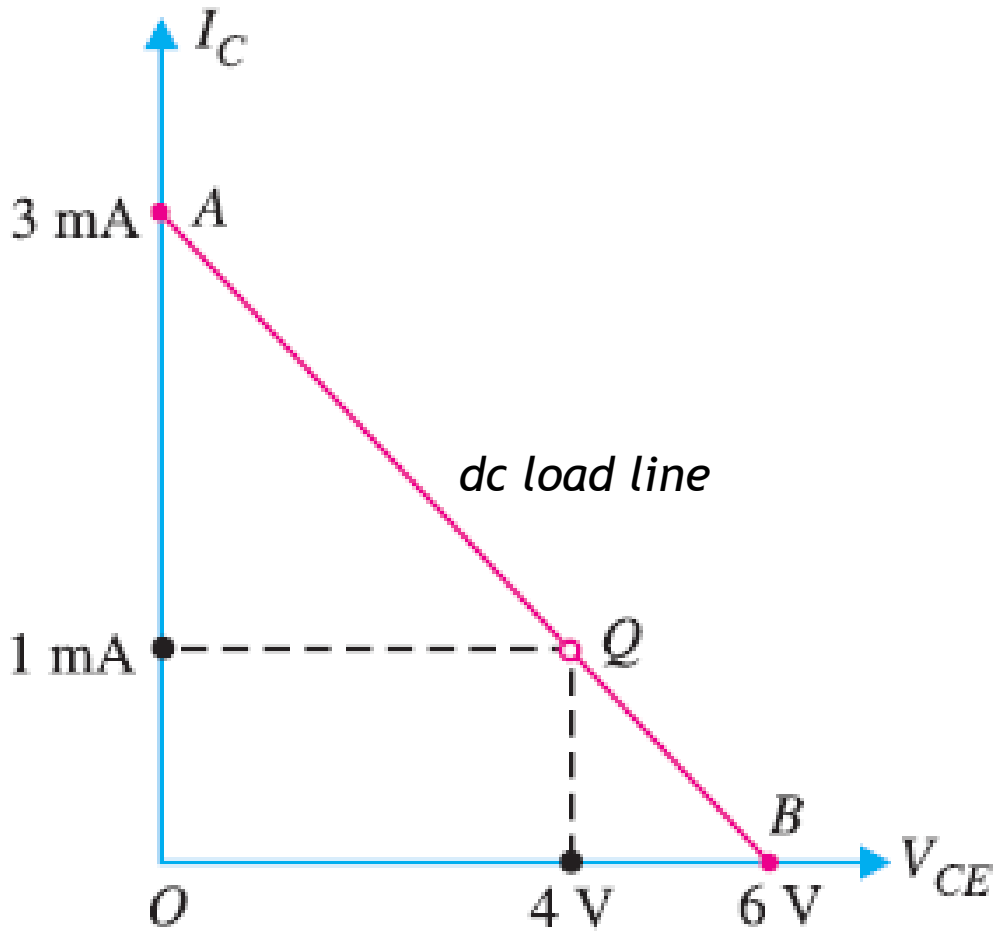
- *Q1. Figure shows that a silicon transistor with β = 100 is biased by base resistor method. Draw the d.c. load line and determine the operating point. What is the stability factor ?*



Base resistor method…

- **Solution:** V_{CC} = 6 V, R_B = 530 kΩ, R_C = 2 kΩ
- **D.C. load line:**
- From above diagram $V_{CE} = V_{CC} - I_C R_C$ *---(1)*
- Put I_C = 0 in equ(1)
- $V_{CE} = V_{CC} - I_C R_C$ => $V_{CE} = V_{CC}$ =6 V *Point B*
- *Put* V_{CE} = 0 in equ(1)
- $0 = V_{CC} - I_C R_C$ => $I_C = V_{CC} / R_C$ =6/2kΩ = 3 mA *Point A*
- *Now draw the dc load line joining points A & B (Next Slide)*

Base resistor method…



Base resistor method…

- **Operating point Q:**
- As it is a silicon transistor, therefore, V_{BE} = 0.7V
- Apply KVL at i/p circuit

$$V_{CC} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{(6 - 0.7)\ \text{V}}{530\ \text{k}\Omega} = 10\ \mu\text{A}$$

$$I_C = \beta I_B = 100 \times 10 = 1000\ \mu\text{A} = 1\ \text{mA}$$

Base resistor method…

$$V_{CE} = V_{CC} - I_C R_C = 6 - 1\ \text{mA} \times 2\ \text{k}\Omega = 6 - 2 = 4\ \text{V}$$

$\therefore$ Operating point is **4 V, 1 mA.**

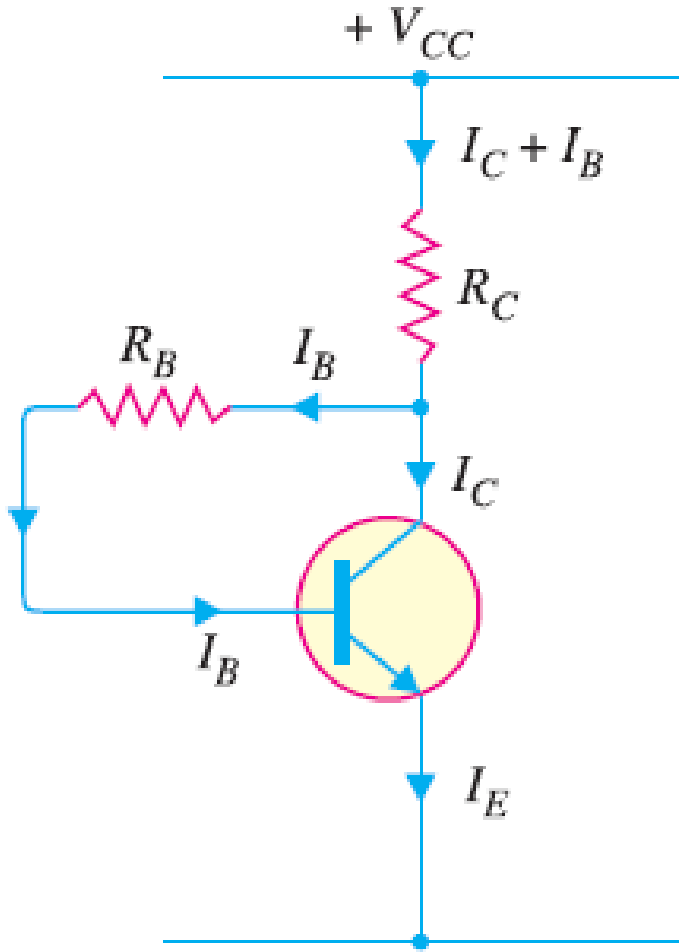
- Operating point (Q) is shown on dc load line
- Stability Factor:

$$S = \beta + 1 = 100 + 1 = \mathbf{101}$$

Emitter Bias Circuit

Biasing with Collector Feedback Resistor

- In this method, one end of R_B is connected to the base and the other end to the collector as shown in figure



Biasing with Collector Feedback Resistor…

- **Circuit analysis:**
- The required value of R_B needed to give the zero signal current I_C can be determined as follows
- $V_{CC} = (I_C+I_B)\, R_C + I_B\, R_B + V_{BE} \approx (I_C)\, R_C + I_B\, R_B + V_{BE}$

[As $I_C >> I_B$ so neglecting]

$$\Rightarrow \quad R_B = \frac{V_{CC} - V_{BE} - I_C R_C}{I_B}$$

$$= \frac{V_{CC} - V_{BE} - \beta\, I_B R_C}{I_B} \qquad (\because I_C = \beta\, I_B)$$

Biasing with Collector Feedback Resistor…

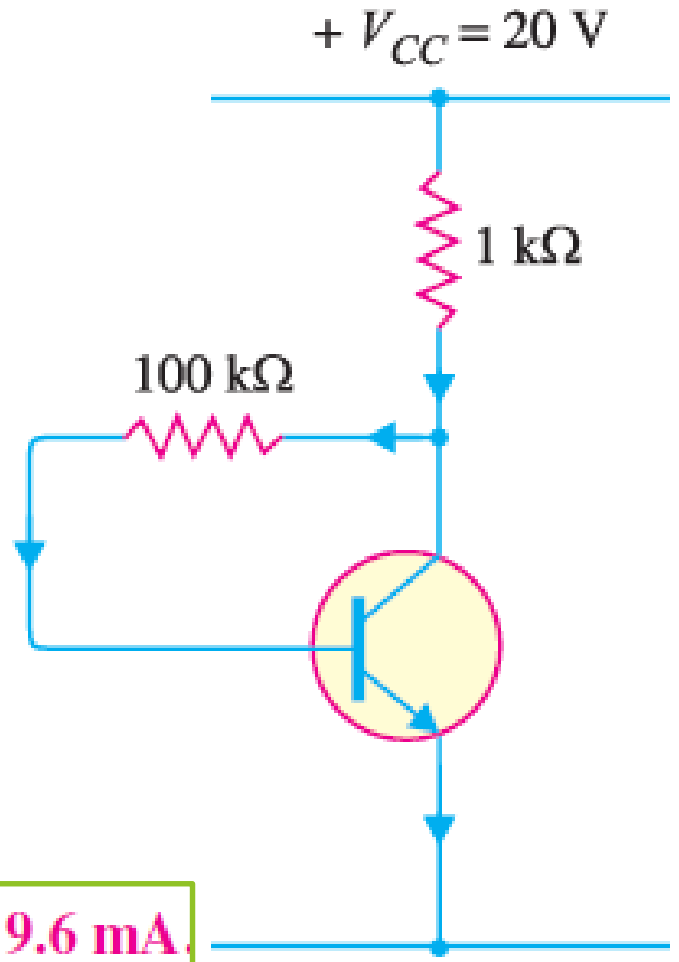
- **Stability factor:** $S < (\beta + 1)$

Biasing with Collector Feedback Resistor…

- **Advantages:**
- (***i***) It is a simple method as it requires only one resistance R_B.
- (***ii***) This circuit provides some stabilisation of the operating point.
- **Disadvantages:**
- (***i***) The circuit does not provide good stabilisation.
- (***ii***) This circuit provides a negative feedback which reduces the gain of the amplifier.

Biasing with Collector Feedback Resistor…

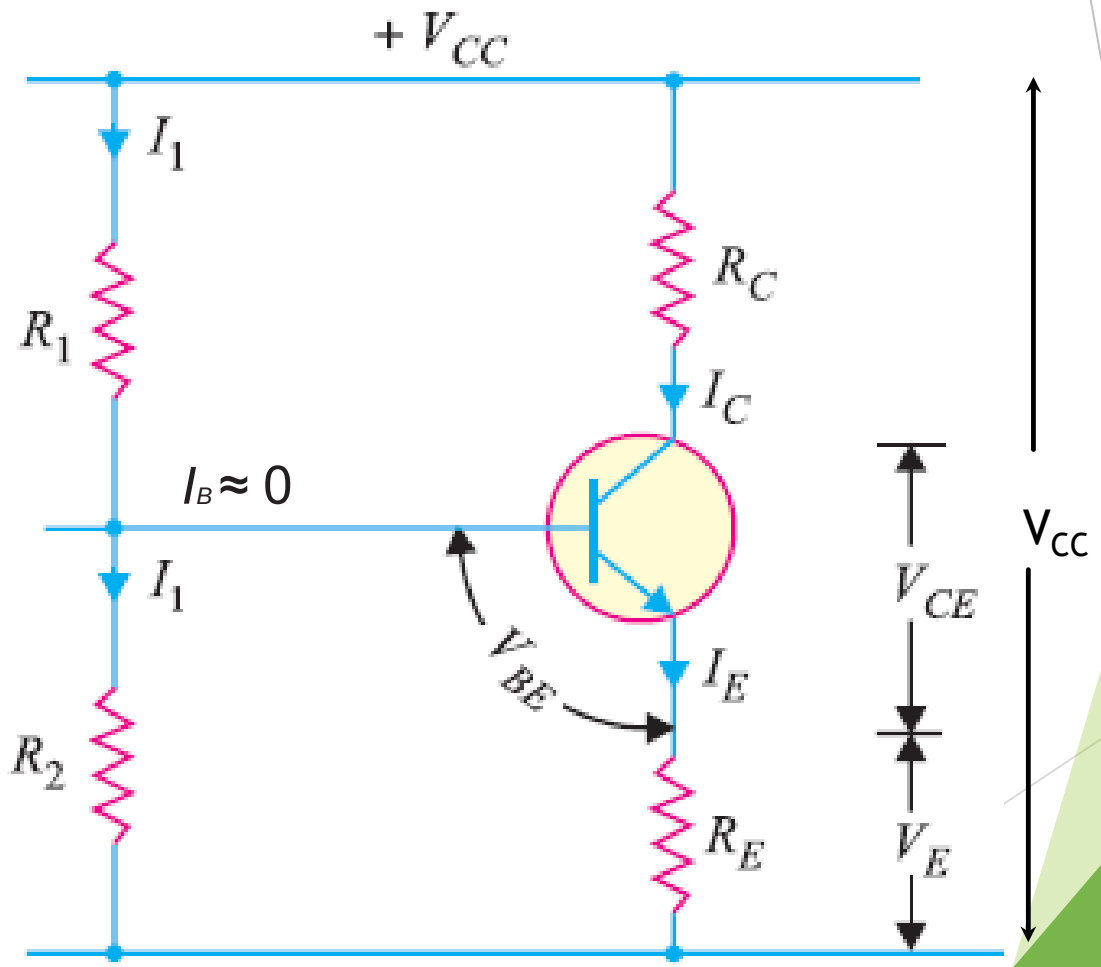
- *Q: Figure shows a silicon transistor biased by collector feedback resistor method. Determine the operating point. Given that β = 100.*



Ans Operating point is **10.4 V, 9.6 mA**.

Voltage Divider Bias Method

- This is the most widely used method.
- In this method, two resistances R_1 and R_2 are connected across the supply voltage V_{CC}.



Voltage Divider Bias Method…

- Circuit analysis:
- (*i*) Collector current IC :

$$I_1 = \frac{V_{CC}}{R_1 + R_2} \Rightarrow \text{Voltage across } R_2, \quad V_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2$$

- Apply KVL to base circuit
- $$V_2 = V_{BE} + V_E \Rightarrow V_2 = V_{BE} + I_E R_E \Rightarrow I_E = \frac{V_2 - V_{BE}}{R_E}$$

$$I_C = \frac{V_2 - V_{BE}}{R_E} \qquad \text{Since } I_E \simeq I_C$$

Voltage Divider Bias Method…

- **(*ii*) Collector-emitter voltage V_{CE}**
- Applying KVL to the collector side
- $V_{CC} = I_C R_C + V_{CE} + I_E R_E$
- $= I_C R_C + V_{CE} + I_C R_E$ (as $I_E \approx I_C$)
- $= I_C (R_C + R_E) + V_{CE}$
- $\therefore V_{CE} = V_{CC} - I_C (R_C + R_E)$

Voltage Divider Bias Method…

- **Stability factor:**

$$S = \frac{(\beta + 1)(R_0 + R_E)}{R_0 + R_E + \beta R_E} \qquad \text{where } R_0 = \frac{R_1 R_2}{R_1 + R_2}$$

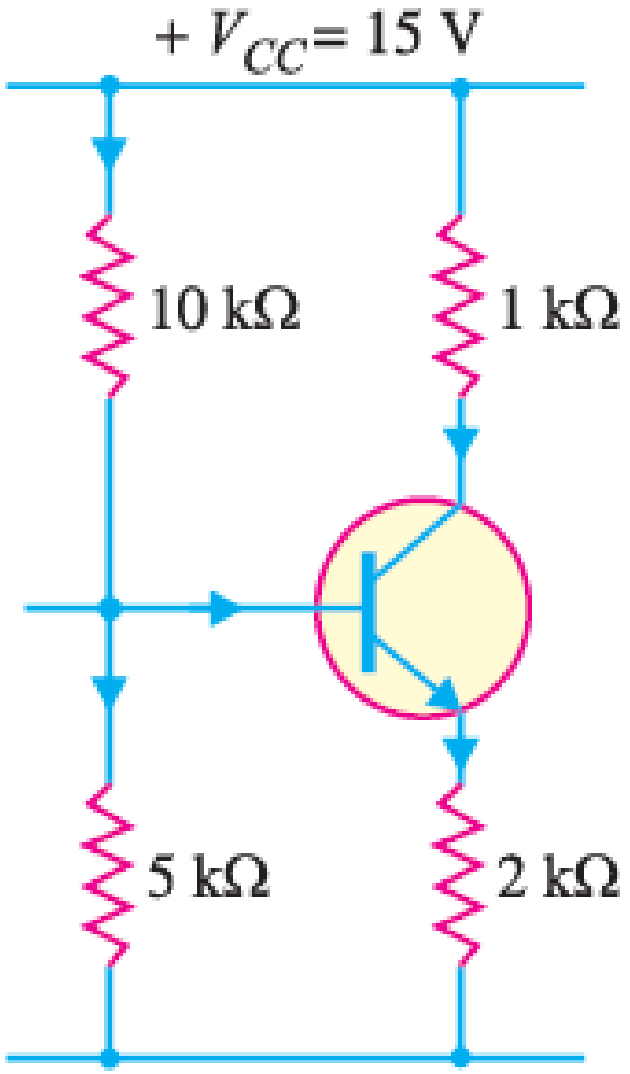
$$= (\beta + 1) \times \frac{1 + \frac{R_0}{R_E}}{\beta + 1 + \frac{R_0}{R_E}}$$

- If the ratio R_0/R_E is very small, then R_0/R_E can be neglected as compared to 1 So

$$\mathbf{S} = (\beta + 1) \times \frac{1}{\beta + 1} = 1$$

Voltage Divider Bias Method…

- Q. Figure *shows the voltage divider bias method. Draw the d.c. load line and determine the operating point. Assume the transistor to be of silicon.*



Voltage Divider Bias Method…

- **Solution:**
- **d.c. load line:**
- The collector-emitter voltage V_{CE} is given by :
- $V_{CE} = V_{CC} - I_C (R_C + R_E)$
- Put $I_C = 0$ in above equ => $V_{CE} = V_{CC} =$ *15 V* *point B*
- *Put $V_{CE} = 0$ in above equ* => $I_C = V_{CC}/(R_C+R_E) = 15/(1+2)K\ \Omega =$ 15 mA Point A
- By joining points *A* and *B*, the d.c. load line *AB* is constructed

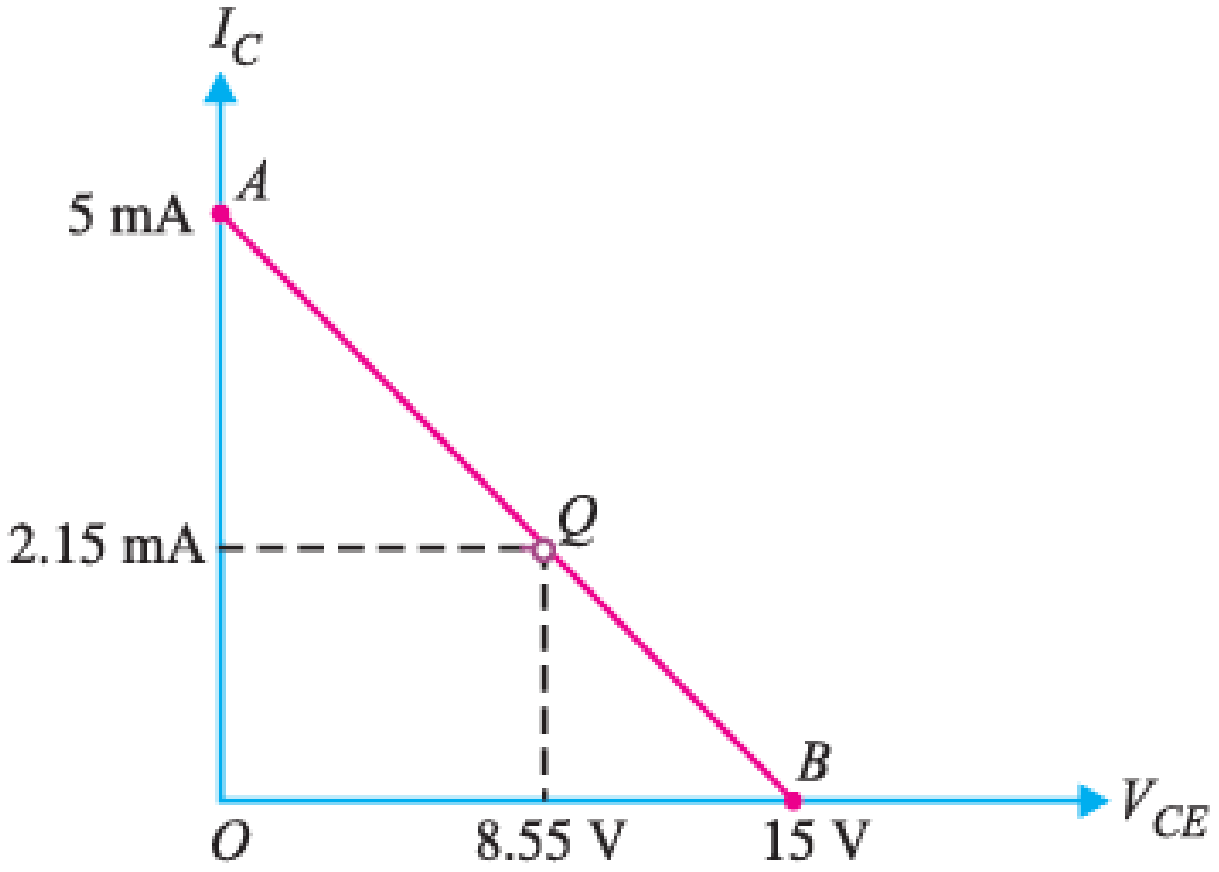
Voltage Divider Bias Method…

- **Operating point:**
- For Si transistor V_{BE} = 0.7 V
- Voltage across 5 kΩ is

$$V_2 = \frac{V_{CC}}{10+5} \times 5 = \frac{15 \times 5}{10+5} = 5 \text{ V}$$

$$I_E = \frac{V_2 - V_{BE}}{R_E} = \frac{5 - 0.7}{2 \text{ k}\Omega} = \frac{4.3 \text{ V}}{2 \text{ k}\Omega} = 2.15 \text{ mA}$$

$$I_C \simeq I_E = 2.15 \text{ mA}$$



Voltage Divider Bias Method…

- Again
- $V_{CE} = V_{CC} - I_C (R_C + R_E)$ Put I_C = 2.15 mA

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$
$$= 15 - 2.15\ \text{mA} \times 3\ \text{k}\Omega = 15 - 6.45 = 8.55\ \text{V}$$

$\therefore$ Operating point is **8.55 V, 2.15 mA.**

- Operating point (Q) is shown on dc load line

Thank you